What is Claimed is:

1. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

etching an underlying gallium nitride layer on a sapphire substrate to selectively expose the sapphire substrate and define at least one post and at least one trench in the underlying gallium nitride layer, the at least one post each including a gallium nitride top and a gallium nitride sidewall, the at least one trench including a sapphire floor; and

laterally growing the gallium nitride sidewall of the at least one post into the at least one trench to thereby form a gallium nitride semiconductor layer.

2. A method according to Claim 1 wherein the etching step comprises the step of:

etching the underlying gallium nitride layer on the sapphire substrate and the sapphire substrate, to define at least one post in the underlying gallium nitride layer and in the sapphire substrate and at least one trench in the underlying gallium nitride layer and in the sapphire substrate, the at least one post each including a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall, the at least one trench including a sapphire floor.

3. A method according to Claim 2 wherein the step of etching comprises the step of etching the sapphire substrate sufficiently deep to prevent vertical growth of gallium nitride from the sapphire floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench.

4. A method according to Claim 2 wherein the sapphire sidewall height to sapphire floor width ratio exceeds about 1/4.

5. A method according to Claim 1 wherein the following step is performed between the steps of etching and laterally growing:

masking the sapphire floor with a mask that reduces nucleation of gallium nitride thereon compared to on sapphire.

6. A method according to Claim 1 wherein the etching step comprises the step of:

etching the underlying gallium nitride layer and an aluminum nitride and/or gallium nitride buffer layer on the sapphire substrate to selectively expose the sapphire substrate and define at least one post in the underlying gallium nitride layer and in the buffer layer and at least one trench in the underlying gallium nitride layer and in the buffer layer, the at least one post including a gallium nitride top, a gallium nitride sidewall and an aluminum nitride sidewall, the at least one trench including a sapphire floor.

7. A method according to Claim 6 wherein the etching step comprises the step of:

etching the underlying gallium nitride layer, the buffer layer on the sapphire substrate and the sapphire substrate to selectively expose the sapphire substrate and define at least one post in the underlying gallium nitride layer, in the buffer layer and in the sapphire substrate, and at least one trench in the underlying gallium nitride layer in the buffer layer and in the sapphire substrate, the at least one post including a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall, the at least one trench including a sapphire floor.

8. A method according to Claim 1 wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

9. A method according to Claim 1:

wherein the step of laterally growing is preceded by the step of masking the gallium nitride top with a mask that reduces nucleation of gallium nitride thereon compared to on gallium nitride; and

wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the mask, to thereby form a gallium nitride semiconductor layer.

10. A method according to Claim 1 wherein the step of laterally growing is followed by the step of forming at least one microelectronic device in the gallium nitride semiconductor layer.

11. A method according to Claim 1 wherein the step of etching is preceded by the step of forming the underlying gallium nitride layer on the sapphire substrate.

12. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

etching an underlying gallium nitride layer on a sapphire substrate to define at least one post in the underlying gallium nitride layer and at least one trench in the underlying gallium nitride layer, the at least one post including a top and a sidewall, the at least one trench including a floor;

masking the at least one floor with a mask; and

laterally growing the sidewall of the at least one post into the at least one trench to thereby form a gallium nitride semiconductor layer.

13. A method according to Claim 12:

wherein the step of etching comprises the step of etching the underlying gallium nitride layer to expose the sapphire substrate and thereby create at least one sapphire floor; and

wherein the step of masking comprises the step of masking the at least one sapphire floor with a mask that reduces nucleation of gallium nitride thereon compared to on sapphire.

14. A method according to Claim 13 further comprising the step of masking the at least one top with a mask.

15. A method according to Claim 14 wherein the steps of masking the at least one floor and masking the at least one top are performed simultaneously.

16. A method according to Claim 12 wherein the step of etching comprises the step of:

etching the underlying gallium nitride layer and an aluminum nitride and/or gallium nitride buffer layer on the sapphire substrate to define at least one post in the underlying gallium nitride layer and in the buffer layer and at least one trench in the underlying gallium nitride layer and the buffer layer, the at least one post including a top and a sidewall, the at least one trench including an aluminum nitride floor.

17. A method according to Claim 12 wherein the step of masking comprises the step of:

etching the underlying gallium nitride layer and an aluminum nitride and/or gallium nitride buffer layer on the sapphire substrate and the sapphire substrate, to define at least one post in the underlying gallium nitride layer, in the buffer layer and in the sapphire substrate and at least one trench in the underlying gallium nitride layer, the buffer layer and the sapphire substrate, the at least one post including a top and a sidewall, the at least one trench including a sapphire floor.

18. A method according to Claim 12 wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

19. A method according to Claim 12:

wherein the step of laterally growing is preceded by the step of masking the gallium nitride top with a mask that reduces nucleation of gallium nitride thereon compared to on gallium nitride; and

wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the mask, to thereby form a gallium nitride semiconductor layer.

20. A method according to Claim 12 wherein the step of laterally growing is followed by the step of forming at least one microelectronic device in the gallium nitride semiconductor layer.

21. A method according to Claim 12 wherein the step of etching is preceded by the step of forming the underlying gallium nitride layer on the sapphire substrate.

22. A method of fabricating a gallium nitride semiconductor layer comprising the steps of:

etching an underlying gallium nitride layer on a sapphire substrate to define at least one post in the underlying gallium nitride layer and at least one trench in the underlying gallium nitride layer, the at least one post including a gallium nitride top, and a gallium nitride sidewall, the at least one trench including a trench floor; and

laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench to thereby form a gallium nitride semiconductor layer;

wherein the laterally growing step is preceded by the step of treating at least one of the sapphire substrate and the underlying gallium nitride layer to prevent vertical growth of gallium nitride from the trench floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench.

23. A method according to Claim 22 wherein the step of treating comprises the step of:

etching the sapphire substrate beneath the at least one trench sufficiently deep to create a sapphire floor and prevent vertical growth of gallium nitride from the sapphire floor from interfering with the step of laterally growing the gallium nitride sidewalls of the at least one post into the at least one trench.

24. A method according to Claim 22 wherein the step of treating comprises the step of:

masking the trench floor with a mask.

25. A method according to Claim 22 wherein the step of treating comprises the step of selectively etching the underlying gallium nitride layer to expose the sapphire substrate and create a sapphire floor.

26. A method according to Claim 22 wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

27. A method according to Claim 22:

wherein the step of laterally growing is preceded by the step of masking the gallium nitride top with a mask that reduces nucleation of gallium nitride thereon compared to on gallium nitride; and

wherein the step of laterally growing comprises the step of laterally overgrowing the gallium nitride sidewall of the at least one post onto the mask, to thereby form a gallium nitride semiconductor layer.

28. A method according to Claim 22 wherein the step of laterally growing is followed by the step of forming at least one microelectronic device in the gallium nitride semiconductor layer.

29. A method according to Claim 22 wherein the step of etching is preceded by the step of forming the underlying gallium nitride layer on the sapphire substrate.

30. A gallium nitride semiconductor structure comprising:

a sapphire substrate;

an underlying gallium nitride layer on the sapphire substrate, the underlying gallium nitride layer including therein at least one post and at least one trench, the at least one post each including a gallium nitride top and a gallium nitride sidewall, the at least one trench including a sapphire floor; and

a lateral gallium nitride layer that extends laterally from the gallium nitride sidewall of the at least one post into the at least one trench.

31. A structure according to Claim 30 wherein the at least one trench extends into the sapphire substrate such that the at least one post each includes a gallium nitride top, a gallium nitride sidewall and a sapphire sidewall and the at least one trench includes a sapphire floor

32. A structure according to Claim 30 wherein the sapphire floor is free of a vertical gallium nitride layer thereon.

33. A structure according to Claim 30 wherein the sapphire sidewall height to sapphire floor width ratio exceeds about 1/4.

34. A structure according to Claim 30 further comprising:

a mask on the sapphire floor.

35. A structure according to Claim 30 further comprising:

an aluminum nitride and/or gallium nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend through the buffer layer.

36. A structure according to Claim 30 wherein the lateral gallium nitride layer further extends onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

37. A structure according to Claim 30 further comprising:

a mask on the gallium nitride top; and

wherein the lateral gallium nitride layer further extends onto the mask, to thereby form a gallium nitride semiconductor layer.

38. A structure according to Claim 30 further comprising at least one microelectronic device in the gallium nitride semiconductor layer.

39. A gallium nitride semiconductor structure comprising:

a sapphire substrate;

an underlying gallium nitride layer on the sapphire substrate, the underlying gallium nitride layer including therein at least one post and at least one trench, the at least one post each including a gallium nitride top and a gallium nitride sidewall, the at least one trench including a trench floor;

a mask on the at least one trench floor; and

a lateral gallium nitride layer that extends laterally from the gallium nitride sidewall of the at least one post into the at least one trench.

40. A structure according to Claim 39:

wherein the trench floor is a sapphire trench floor.

41. A structure according to Claim 39 wherein the mask is a first mask, the structure further comprising:

a second mask on the gallium nitride top.

42. A structure according to Claim 41 wherein the first mask and the second mask comprise same material.

43. A structure according to Claim 39 further comprising an aluminum nitride buffer and/or gallium nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend into the buffer layer.

44. A structure according to Claim 39 further comprising an aluminum nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend through the buffer layer.

45. A structure according to Claim 39 further comprising an aluminum nitride buffer layer between the sapphire substrate and the underlying gallium nitride layer, wherein the at least one post and the at least one trench extend through the buffer layer and into the sapphire substrate.

46. A structure according to Claim 39 wherein the lateral gallium nitride layer further extends onto the gallium nitride top, to thereby form a gallium nitride semiconductor layer.

47. A structure according to Claim 39 wherein the mask is a first mask, the structure further comprising:

a second mask on the gallium nitride top; and

wherein the lateral gallium nitride layer further extends onto the mask, to thereby form a gallium nitride semiconductor layer.

48. A structure according to Claim 39 further comprising at least one microelectronic device in the gallium nitride semiconductor layer.